

Features

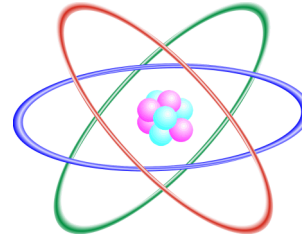
- Fully programmable coefficient FIR filter.
- Filter order (length) up to 4096 points (taps).
- Real or complex data.
- Data, coefficient, output, and arithmetic precision up to 128 bits.
- Filter sample rate 300+ MSa/s (*three hundred million* samples per second).
- Implementation is synchronous with a single clock domain.
- High-level simulation models (HDL, Athena Siglab XL) are available.
- Portable to external technologies.

Benefits

- Exceeds DSP microprocessor performance by orders of magnitude at much lower cost.
- Lowest power per computation.
- No instruction set processor overhead.
- Example: 32 tap filter at 100 MSa/s generates 3.2 billion multiply-accumulates per second using ~52K gates at 125 mW.
- Programmable coefficients lower design risk.

Applications

- RF/IF signal processing.
- Correlation/matched filtering.
- Programmable and/or adaptive channel equalization.
- Signal pre-processor between ADC and other processing.
- Microprocessor accelerator.



Athena Programmable FIR Filter Atomic DSP Family

Description

The standard version of this high-performance, programmable coefficient FIR filter ranges from three to 4096 taps and accepts user defined input data, coefficient, output, and arithmetic precision up to 128 bits. (Longer filters and higher precision are available.) The filter operates on both real and complex data. Coefficients, programmed serially at a rate of up to one/clock cycle, may be real or complex. The filter accepts and produces up to 1 input/output sample per clock cycle and may be configured as either free running or controlled by either a single register enable or a bubble compressing pipeline controller. The filter operates normally at speeds up to 300 MSa/s and, with architectural restrictions, may achieve speeds in excess of 500 MSa/s.

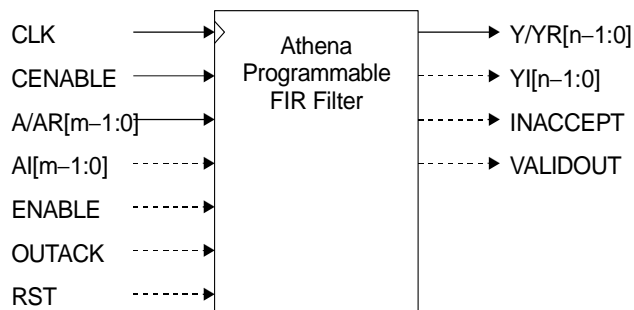


Figure 1: Athena Programmable FIR Block Diagram

Operation

Figure 1 shows a block diagram of the Athena programmable FIR filter.

Atomic DSP Family

Incredibly small and power efficient, the entire family of Athena digital signal processing (DSP) accelerator cores is designed specifically for computationally intensive system-on-a-chip applications. Additional products are in development for the wireless and broadband communications markets. These new processors will join Athena's complete DSP semiconductor IP library designed for power-sensitive applications requiring extraordinary performance.

Delivery

Each Atomic DSP core package is delivered as a firm core optimized to any customer-specified library. The package includes the core, verification suites, timing and simulation models, and documentation.

Athena's IP cores are designed for efficient implementation and rapid delivery. The company's proprietary, wholly automated implementation and verification methodology produces synchronous, testable IP cores of the highest quality. All Athena IP cores achieve a score of 95% or better on the OpenMore scale of IP reusability.

About The Athena Group, Inc.

The Athena Group, Inc. of Gainesville, Florida licenses high-performance DSP technology that delivers breakthrough performance, reduced area, and lower power consumption in a broad range of SoC products. Athena's proprietary technology powers leading edge applications such as secure e-commerce, wireless communications, and video compression. In addition to their high-value application level solutions, Athena also produces a full line of fundamental DSP functions suitable for SoC integration.

Athena was founded in 1986 and is privately held.



The Athena Group, Inc.
5522 NW 43rd Street, Suite B
Gainesville, FL 32653

Phone: (352) 371-2567
Toll-free: (800) 741-7440
Fax: (352) 373-5182
www.athena-group.com

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