

Features

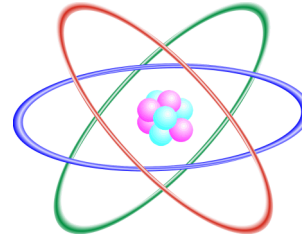
- FFTs up to 64K (65,536) points.
- User selectable transform size at run time.
- Integrated data pre-multiplier.
- Input data precision 4 to 16 bits.
- Output data precision 4 to 32 bits.
- High-speed performance:
 - up to 195K 512 point transforms per second (5 ms/transform)
 - up to 18.3K 4096 point transforms per second (54.6 ms/transform)
- Synchronous implementation with a single clock domain.

Benefits

- Modulate/demodulate up to 45 full-rate ADSL channels per processor.
- Lower power/computation than microprocessor and no instruction set overhead.
- Better power, performance characteristics than microprocessors.

Applications

- Modulation and demodulation for discrete multi-tone (DMT) communications (e.g., ADSL).
- Frequency excision filtering of co-channel interference (CCI) sources for communications receivers (e.g., GPS).
- Spectrum analysis.
 - Psycho-acoustic analysis for real-time MP3 encoding.
 - Signal detection.
- Cross-correlation.



Athena Combined FFT/IFFT Processor Atomic DSP Family

Description

The Athena Fast Fourier Transform (FFT)/Inverse FFT template produces a high-performance processor which executes FFTs and IFFTs on both real and complex data records ranging from eight to 64K (65,536) points. The Athena FFT/IFFT processor incorporates a multiplier used to window or mask data records in both the time/spatial and frequency domains.

The Athena FFT/IFFT processor may be integrated with a signal processing data path or as a microprocessor accelerator. When attached to a microprocessor (e.g., ARM9 via AMBA AHB) and operating at full speed on 512 point transforms, the Athena FFT/IFFT accelerator provides the equivalent of approximately 1.8 billion multiply-accumulates per second.

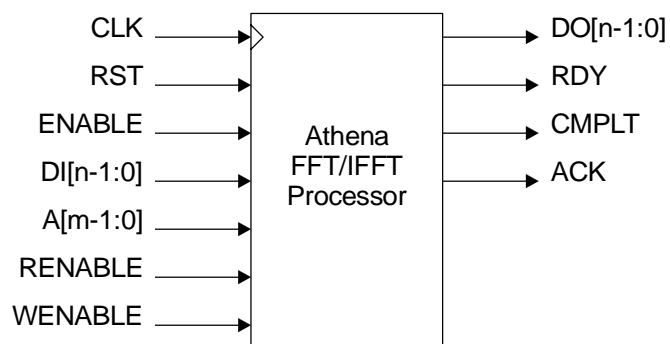


Figure 1: Athena Combined FFT/IFFT Processor Block Diagram

Operation

Figure 1 shows a block diagram of the Athena Combined FFT/IFFT processor.

Atomic DSP Family

Incredibly small and power efficient, the entire family of Athena digital signal processing (DSP) accelerator cores is designed specifically for computationally intensive system-on-a-chip applications. Additional products are in development for the wireless and broadband communications markets. These new processors will join Athena's complete DSP semiconductor IP library designed for power-sensitive applications requiring extraordinary performance.

Delivery

Each Atomic DSP core package is delivered as a firm core optimized to any customer-specified library. The package includes the core, verification suites, timing and simulation models, and documentation.

Athena's IP cores are designed for efficient implementation and rapid delivery. The company's proprietary, wholly automated implementation and verification methodology produces synchronous, testable IP cores of the highest quality. All Athena IP cores achieve a score of 95% or better on the OpenMore scale of IP reusability.

About The Athena Group, Inc.

The Athena Group, Inc. of Gainesville, Florida licenses high-performance DSP technology that delivers breakthrough performance, reduced area, and lower power consumption in a broad range of SoC products. Athena's proprietary technology powers leading edge applications such as secure e-commerce, wireless communications, and video compression. In addition to their high-value application level solutions, Athena also produces a full line of fundamental DSP functions suitable for SoC integration.

Athena was founded in 1986 and is privately held.



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